METHOD FOR FORMING A METAL SILICIDE LAYER IN A SEMICONDUCTOR DEVICE

ABSTRACT OF THE DISCLOSURE

On first and second regions of a substrate are formed a first gate structure including a first gate electrode and a first spacer, and a second gate structure including a second gate electrode and a second spacer, respectively. The first and second spacers are removed to different depths such that side portions of the first and second gate electrodes have different exposed thicknesses. A metal silicide layer is formed on the first and second regions including the first and second gate structures. The metal silicide layer formed on the second gate electrode has a second thickness that is greater than a first thickness of the metal silicide layer formed on the first gate electrode. The spacers in the gate structures of resulting N type and P type MOS transistors are removed to different thicknesses, thereby minimizing deformation in the gate structures and also improving electrical characteristics and thermal stability of the gate electrodes.